REMARKS/ARGUMENTS

In the above-identified Office Action, the Examiner has allowed Claims 17-25 with some objections as to form. The applicants believe they have adequately addressed these objections herein.

Additionally, Claims 1-8, 31-32, and 39 are rejected under 35 U.S.C. §103(a) in view of various references. The pending objections and rejections are discussed below.

In this amendment, **Claim 17 is amended** and **Claims 31 and 32 are cancelled**. Also, **Claims 9-16, 26-30, and 33-38 were previously** cancelled. Accordingly, Claims 1-8, 17-25, and 39 remain pending in this application.

Reconsideration of the application is respectfully requested based on the amendments and the following remarks.

Objections to the Claims

Claim 31 has been objected to. Applicants have cancelled Claim 31. Thus, it is respectfully submitted that there is no longer any need to amend claim 31.

Claim 17 has been amended to address the objections as to form raised by the Examiner. The applicants respectfully submit that the amendments made address the Examiners concerns regarding the claimed invention.

Accordingly, applicants respectfully request that the objections to all pending claims be removed.

Allowed Claims 17-25

The applicants thank the Examiner for his kind indication of allowability as to **Claims 17-25. Claims 17-25** pertain to a microprocessor and system claimed in accordance with aspects of the invention. The objected to portions of Claim 17 have been corrected as requested by the Examiner. Accordingly, it is now submitted that Claims 17-25 are all in condition for allowance and applicants request that the pending objections be removed.

Art Based Rejections

In the Office Action, the Examiner rejected **claims 1-8 & 39** under 35 U.S.C. §103(a) as

being unpatentable over Bartley (U.S. Patent No. 6,219,796, hereinafter "*Bartley*") in view of Fletcher et al. (U.S. Patent No. 6,611,920, hereinafter "*Fletcher*"); rejected **claims 31 and 32** over *Bartley* in view of *Fletcher* and *Sproch*; and rejected **claim 39** over *Bartley, Fletcher*, and *Simonvich* (U.S. Patent 6,308,241, hereinafter "*Simonvich*"). These rejections are discussed below.

Claims 31 & 32

Claims 31 and 32 have been canceled making a discussion of these claims moot at this time. Accordingly, it is respectfully requested that the Examiner withdraw the rejections of Claims 31 & 32 which are no longer pending in the application.

Rejections Under 35 U.S.C. § 103

Discussion of Claims 1-8 & 39

Claims 1-8 stand rejected as unpatentable under 35 U. S. C. §§ 103(a) over *Bartley* in view of *Fletcher*.

The Action offers (for example, at item 5, on page 1) that *Bartley* teaches a "microprocessor including a functional unit [11] formed of a plurality of stages [functional units]. This statement is perhaps at the heart of the differences between the claimed invention and the cited art. The term "functional unit" means something different in *Bartley* than it does in the claimed invention. Item 11 of *Bartley* is not a "functional unit" but, rather a CPU core *containing* functional unit blocks, or more importantly, datapaths (11d or 11e) that each contain several functional units (e.g., L1, S1, M1, D1, See, also *Bartley* at 5:35-40) that perform specific operations on selected instruction types. Thus, the *Bartley* functional blocks refer to a higher level in the processing hierarchy than the claimed "functional blocks" of the claimed invention. The functional blocks of the present invention are akin to the blocks L1, S1, M1, D1 of *Bartley*. Reference to *Bartley* at, for example, 5:35-40 confirms this. The *Bartley* functional units (e.g., L1, S1, M1, D1) are not sequentially operating stages of a functional unit, but rather are parallel functional units such as depicted in the present invention (See, e.g., 106 of Fig. 1 or 302 of Fig. 3 and so on). This is a seriously important distinction which the applicants wish to explain.

As is known to those having ordinary skill in the art, when a functional unit processes an instruction it executes the instruction using a sequential process of a series of "stages" that when completed comprise the full execution of the instruction by the functional unit. All of the cited references discuss the operation and control of power to entire functional units. None of the

references discuss selective control of power to the specific stages that make up the functional units. The stages are not depicted in *Bartley*. In actuality, the stages would describe how *Bartley's* functional units (e.g., L1, S1, M1, D1) operate. Thus, the claimed invention operates at a more granular level than the cited art. *Bartley* does not describe how portions (the stages) of L1 or S1 and so on can be turned on and off. Instead all of these functional units are turned off in their entirety when power saving is needed instead of selectively turning off the stages of L1 or S1 as they are not needed.

Particularly adding to this confusion is the *Bartley's* misuse of the term "functional unit". This is explained as follows. Item 11 of *Bartley* is a CPU, not a functional unit as the Action would have it. Accordingly, this misinterpretation misconstrues *Bartley*. In *Bartley* the core contains functional unit blocks, or more importantly, datapaths (11d or 11e) that each contain several functional units (e.g., L1, S1, M1, D1, See, also Bartley at 5:35-40) that perform specific operations on selected instruction types. These are the functional units described in the present invention and the cited art. Thus, the functional units (e.g., L1, S1, M1, D1) are not sequentially operating stages of a functional unit as the Office Action uses the term, but rather are parallel functional units such as depicted in the present invention (See, e.g., 106 of Fig. 1 or 302 of Fig. 3 and so on). Even *Bartley* depicts them so (see for example, FIG. 1 of *Bartley*).

Moreover, *Bartley* does not depict or otherwise describe the stage operation of any of the functional units. The cited portions of *Bartley* (3:1-30 and 3:41-65) describe a process for shutting down of entire functional units (See, e.g., Bartley at 5:50-60). *Bartley* selectively turns these functional units on and off to save power when the functional units are not needed. This is a rough method of power control. The specification of the instant application describes this pre-existing methodology in some degree of detail. Accordingly, *Bartley* has absolutely no applicability to the present invention and is not properly employed in an obviousness type rejection. The cited art discloses no understanding of the fact that even though a functional unit can be "on", power can still be saved by selectively turning off the power to selected stages of the "on" functional unit. This is a radical departure from the prior art. The same lack of granular power control is also present in *Fletcher* (see, for example, 3:47-52). The present specification goes into great detail describing precisely the limitations of methodologies like that of *Bartley* and *Fletcher*.

An advantage of the present invention is explained as follows. During the operation of a functional unit the instruction passes through a sequence of stages used to execute the instruction using the functional unit (Figs. 5, 6A-6E illustrate this). The instruction is processed

sequentially through each of these stages using a clocked sequence of steps that advance the processing in accord with the clock pulses of the microprocessor. Thus, the functional unit executes a series of steps (stages) during the time the functional unit uses to process a given instruction. The inventors have noted that when an instruction is processed by a functional unit, for most of the stages, no operations are required. They have also determined that the various stages of a functional unit can be turned off without turning off all power to the entire functional unit. Thus, other stages still in use are powered while the power is off to the stages not processing (for example, those processing no-op's instruction steps). This allows power to be selectively supplied to only the needed stages and the non-operational stages go without power. This allows finer granularity of power control and saves even more power than the ideas suggested by *Bartley* and *Fletcher*.

Thus, both the cited portions of *Fletcher* and *Bartley* describe systems for turning off entire functional units instead of turning the stages on and off.

Specifically, **Claim 1** of the present invention requires the "stages of said functional unit are arranged in series" and controlling of the supply of current to each of a plurality of stages of a functional unit after evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. The method of claim 1 allows for efficient evaluation of operation type of each instruction so that power supplied to each stage of a functional unit can be individually controlled. This is done "by providing a clock signal and the activity indicators to a logic gate that determines that only selected stages of said plurality of stages will draw current from a power supply". The cited art fails to teach or suggest these limitations.

Accordingly, it is submitted that *Fletcher* and *Bartley* alone or in any combination, do not teach or suggest all the features of Claim 1. In addition, it is submitted that dependent claims 2-8 are also patentably distinct from cited art for at least the same reasons as those recited above for independent Claim 1. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-8.

Claim 39 is rejected as unpatentable under 35 U. S. C. §§ 103(a) over *Fletcher, Bartley* and *Simonovich*. Much the same shortcomings are expressed with respect to Claim 39 as were present in the discussion of Base Claim 1. The addition of *Simonovich* does not correct the underlying shortcomings of *Fletcher* and *Bartley*. Accordingly, it is submitted that *Fletcher, Bartley* and *Simonovich* alone or in any combination, do not teach or suggest all the features of

Claim 39. Due to the underlying deficiency of *Fletcher* and *Bartley* it is respectfully submitted that the additional limitations recited in Claim 39 need not be discussed. Thus, it is respectfully requested that the Examiner withdraw the rejection of Claim 39.

Thus, it is respectfully requested that the Examiner withdraw the rejection of pending Claims 1-8 and 39 under 35 U.S.C § 103(a).

Conclusion:

In view of the foregoing amendments and remarks, it is respectfully submitted that the claimed invention as presently presented is patentable over the art of record and that this case is now in condition for allowance.

Accordingly, the applicants request withdrawal of all pending rejections and request reconsideration of the pending application and prompt passage to issuance. As an aside, the applicants clarify that any lack of response to any of the issues raised by the Examiner is not an admission by the applicant as to the accuracy of the Examiner's assertions with respect to such issues. Accordingly, applicant's specifically reserve the right to respond to such issues at a later time during the prosecution of the present application, should such a need arise.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Additionally, if any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. APL1P203).

Respectfully submitted,

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